



## GENERAL DESCRIPTION

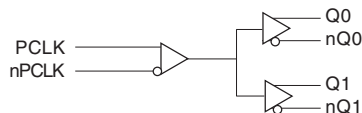


The ICS853011 is a low skew, high performance 1-to-2 Differential-to-2.5V/3.3V LVPECL/ECL Fanout Buffer and a member of the HiPerClockSTM family of High Performance Clock Solutions from ICS. The ICS853011 is characterized to operate from either a 2.5V or a 3.3V power supply. Guaranteed output and part-to-part skew characteristics make the ICS853011 ideal for those clock distribution applications demanding well defined performance and repeatability.

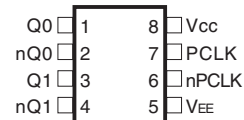
## FEATURES

- 2 differential 2.5V/3.3V LVPECL / ECL outputs
- 1 differential PCLK, nPCLK input pair
- PCLK, nPCLK pair can accept the following differential input levels: LVPECL, LVDS, CML, SSTL
- Maximum output frequency: >3GHz
- Translates any single ended input signal to 3.3V LVPECL levels with resistor bias on nPCLK input
- Output skew: 5ps (typical)
- Part-to-part skew: 130ps (maximum)
- Propagation delay: 390ps (maximum)
- Additive phase jitter, RMS: 0.06ps (typical)
- LVPECL mode operating voltage supply range:  
 $V_{CC} = 2.375V$  to  $3.8V$ ,  $V_{EE} = 0V$
- ECL mode operating voltage supply range:  
 $V_{CC} = 0V$ ,  $V_{EE} = -3.8V$  to  $-2.375V$
- $-40^{\circ}C$  to  $85^{\circ}C$  ambient operating temperature
- Available in both Standard and lead-free RoHS compliant packages

## BLOCK DIAGRAM



## PIN ASSIGNMENT



**ICS853011**  
**8-Lead SOIC**

3.90mm x 4.90mm x 1.37mm package body

**M Package**  
Top View

**ICS853011**  
**8-Lead TSSOP, 118 mil**

3mm x 3mm x 0.95mm package body

**G Package**  
Top View



**TABLE 1. PIN DESCRIPTIONS**

Number	Name	Type		Description
1, 2	Q0, nQ0	Output		Differential output pair. LVPECL interface levels.
3, 4	Q1, nQ1	Output		Differential output pair. LVPECL interface levels.
5	V <sub>EE</sub>	Power		Negative supply pin.
6	nPCLK	Input	Pullup/ Pulldown	Clock input. V <sub>CC</sub> /2 default when left floating. LVPECL interface levels.
7	PCLK	Input	Pulldown	Clock input. Default LOW when left floating. LVPECL interface levels.
8	V <sub>CC</sub>	Power		Positive supply pin.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			75		kΩ
R <sub>VCC/2</sub>	Pullup/Pulldown Resistors			50		kΩ



#### ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $V_{CC}$	4.6V (LVPECL mode, $V_{EE} = 0$ )
Negative Supply Voltage, $V_{EE}$	-4.6V (ECL mode, $V_{CC} = 0$ )
Inputs, $V_I$ (LVPECL mode)	-0.5V to $V_{CC} + 0.5V$
Inputs, $V_I$ (ECL mode)	0.5V to $V_{EE} - 0.5V$
Outputs, $I_o$	
Continuous Current	50mA
Surge Current	100mA
Operating Temperature Range, $T_A$	-40°C to +85°C
Storage Temperature, $T_{STG}$	-65°C to 150°C
Package Thermal Impedance, $\theta_{JA}$	112.7°C/W (0 lfpm)
(Junction-to-Ambient) for 8 Lead SOIC	
Package Thermal Impedance, $\theta_{JA}$	101.7°C/W (0 m/s)
(Junction-to-Ambient) for 8 Lead TSSOP	

**NOTE:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 3A. POWER SUPPLY DC CHARACTERISTICS,  $V_{CC} = 2.375V$  TO  $3.8V$ ;  $V_{EE} = 0V$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Positive Supply Voltage		2.375	3.3	3.8	V
$I_{EE}$	Power Supply Current				25	mA

**TABLE 3B. LVPECL DC CHARACTERISTICS,  $V_{CC} = 3.3V$ ;  $V_{EE} = 0V$**

Symbol	Parameter	-40°C			25°C			85°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$V_{OH}$	Output High Voltage; NOTE 1	2.175	2.275	2.38	2.225	2.295	2.37	2.22	2.295	2.365	V
$V_{OL}$	Output Low Voltage; NOTE 1	1.405	1.545	1.68	1.425	1.52	1.615	1.44	1.535	1.63	V
$V_{PP}$	Peak-to-Peak Input Voltage	150	800	1200	150	800	1200	150	800	1200	V
$V_{CMR}$	Input High Voltage Common Mode Range; NOTE 2, 3	1.2		3.3	1.2		3.3	1.2		3.3	V
$I_{IH}$	Input High Current	PCLK, nPCLK		150			150			150	μA
$I_{IL}$	Input Low Current	PCLK		-10			-10			-10	μA
		nPCLK		-150			-150			-150	μA

Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.925V to -0.5V.

NOTE 1: Outputs terminated with 50Ω to  $V_{CC} - 2V$ .

NOTE 2: Common mode voltage is defined as  $V_{IH}$ .

NOTE 3: For single-ended applications, the maximum input voltage for PCLK, nPCLK is  $V_{CC} + 0.3V$ .



**TABLE 3C. LVPECL DC CHARACTERISTICS,  $V_{CC} = 2.5V$ ;  $V_{EE} = 0V$**

Symbol	Parameter	-40°C			25°C			85°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$V_{OH}$	Output High Voltage; NOTE 1	1.375	1.475	1.58	1.425	1.495	1.57	1.42	1.495	1.565	V
$V_{OL}$	Output Low Voltage; NOTE 1	0.605	0.745	0.88	0.625	0.72	0.815	0.64	0.735	0.83	V
$V_{PP}$	Peak-to-Peak Input Voltage	150	800	1200	150	800	1200	150	800	1200	V
$V_{CMR}$	Input High Voltage Common Mode Range; NOTE 2, 3	1.2		2.5	1.2		2.5	1.2		2.5	V
$I_{IH}$	Input High Current	PCLK, nPCLK		150			150			150	$\mu A$
$I_{IL}$	Input Low Current	PCLK		-10			-10			-10	$\mu A$
		nPCLK		-150			-150			-150	$\mu A$

For notes see above Table 3B, 3.3V LVPECL DC Characteristics.

**TABLE 3D. ECL DC CHARACTERISTICS,  $V_{CC} = 0V$ ;  $V_{EE} = -3.8V$  TO  $-2.375V$**

Symbol	Parameter	-40°C			25°C			85°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$V_{OH}$	Output High Voltage; NOTE 1	-1.125	-1.025	-0.92	-1.075	-1.005	-0.93	-1.08	-1.005	-0.935	V
$V_{OL}$	Output Low Voltage; NOTE 1	-1.895	-1.755	-1.62	-1.875	-1.78	-1.685	-1.86	-1.765	-1.67	V
$V_{PP}$	Peak-to-Peak Input Voltage	150	800	1200	150	800	1200	150	800	1200	V
$V_{CMR}$	Input High Voltage Common Mode Range; NOTE 2, 3	$V_{EE}+1.2V$		0	$V_{EE}+1.2V$		0	$V_{EE}+1.2V$		0	V
$I_{IH}$	Input High Current	PCLK, nPCLK		150			150			150	$\mu A$
$I_{IL}$	Input Low Current	PCLK		-10			-10			-10	$\mu A$
		nPCLK		-150			-150			-150	$\mu A$

Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.925V to -0.5V.

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CC} - 2V$ .

NOTE 2: Common mode voltage is defined as  $V_{IH}$ .

NOTE 3: For single-ended applications, the maximum input voltage for PCLK, nPCLK is  $V_{CC} + 0.3V$ .

**TABLE 4. AC CHARACTERISTICS,  $V_{CC} = 0V$ ;  $V_{EE} = -3.8V$  TO  $-2.375V$  OR  $V_{CC} = 2.375$  TO  $3.8V$ ;  $V_{EE} = 0V$**

Symbol	Parameter	-40°C			25°C			85°C			Units		
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
$f_{MAX}$	Output Frequency			>3			>3			>3	GHz		
$t_{PD}$	Propagation Delay; NOTE 1	245		375	260		390	275		415	ps		
$t_{sk(o)}$	Output Skew; NOTE 2, 4		5	20		5	20		5	20	ps		
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 3, 4			130			130			150	ps		
$f_{jit}$	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section, Integration Range: 12KHz to 20MHz		0.06			0.06			0.06		ps		
$t_R/t_F$	Output Rise/Fall Time	20% to 80%		70		250	80		250	100		250	ps
odc	Output Duty Cycle	$f \leq 1GHz$		48	50	52	48	50	52	48	50	52	%

All parameters are measured at  $f \leq 1.7GHz$ , unless otherwise noted.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.

Measured at the output differential cross points.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

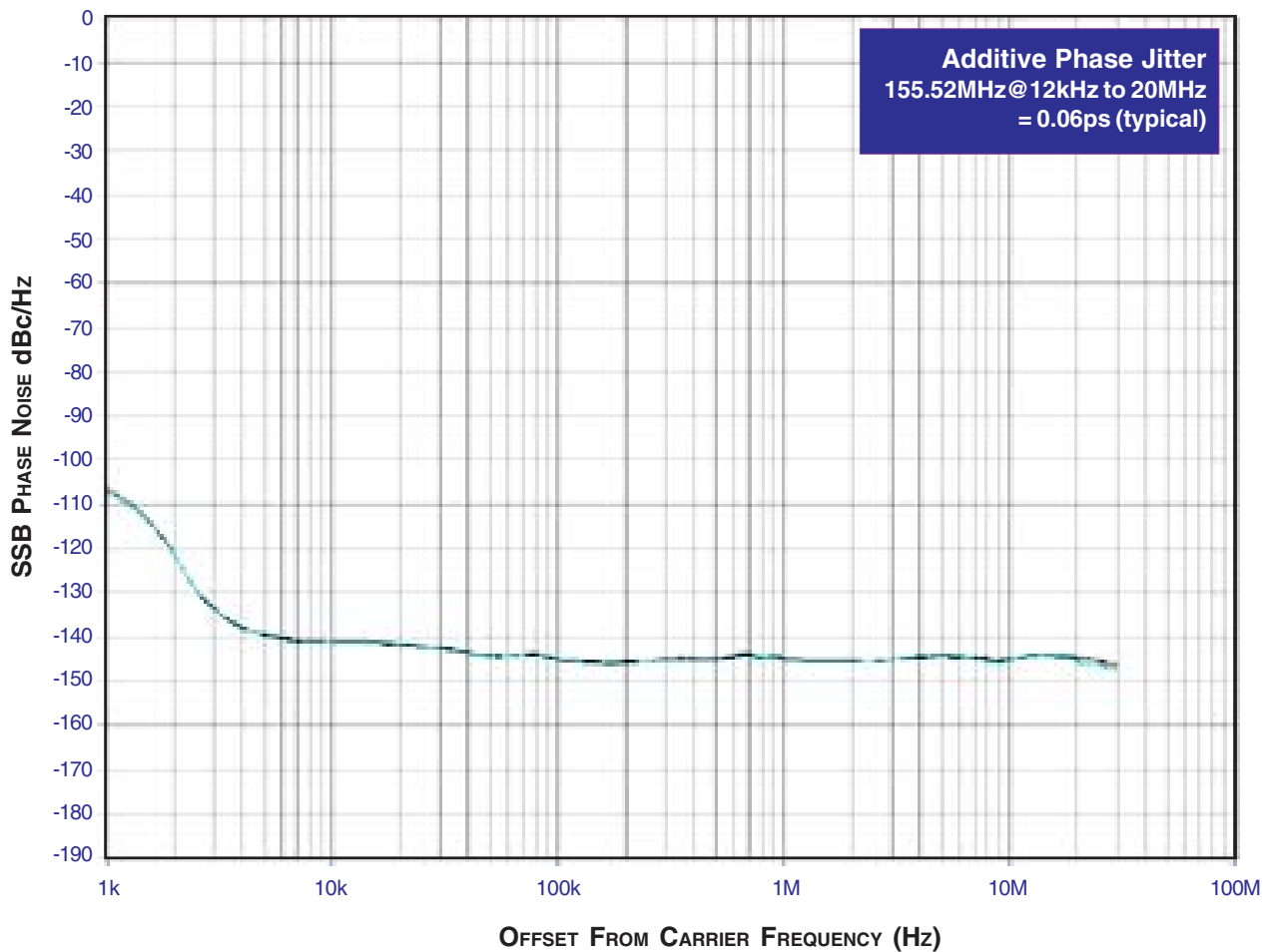
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.



### ADDITIVE PHASE JITTER

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the **dBc Phase Noise**. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in

the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a **dBc** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

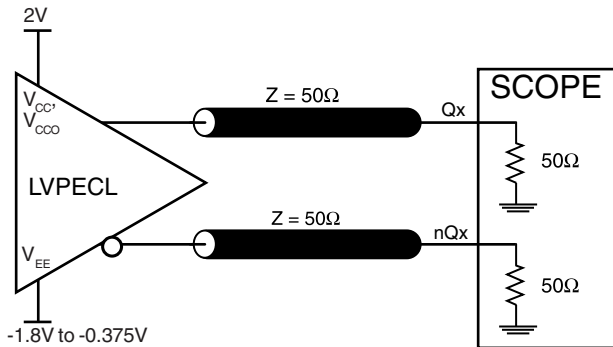


As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The de-

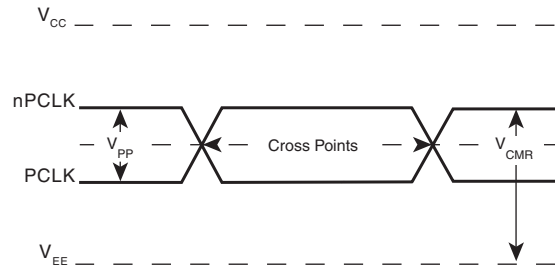
vice meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.



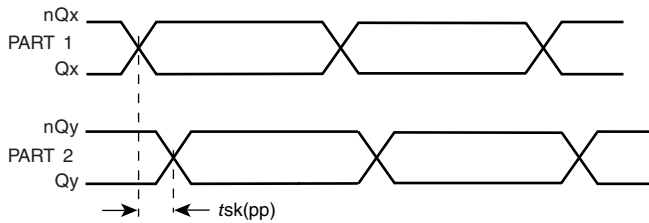
## PARAMETER MEASUREMENT INFORMATION



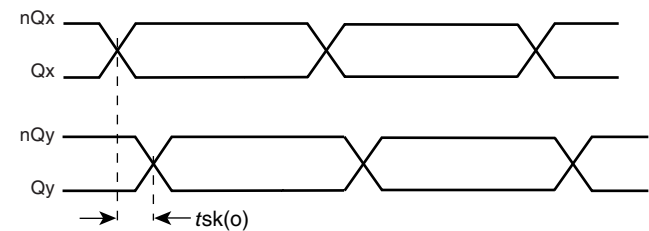
**OUTPUT LOAD AC TEST CIRCUIT**



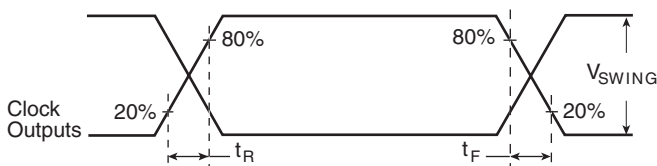
**DIFFERENTIAL INPUT LEVEL**



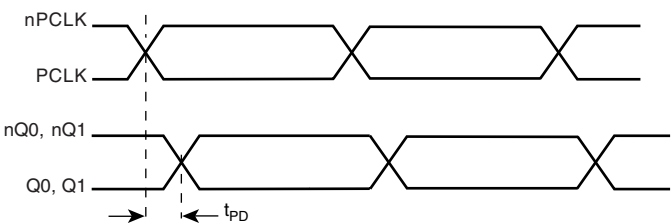
**PART-TO-PART SKEW**



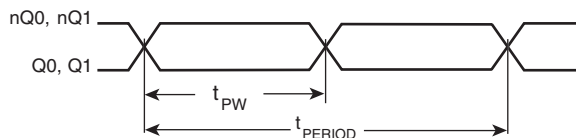
**OUTPUT SKEW**



**OUTPUT RISE/FALL TIME**



**PROPAGATION DELAY**



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

**OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD**

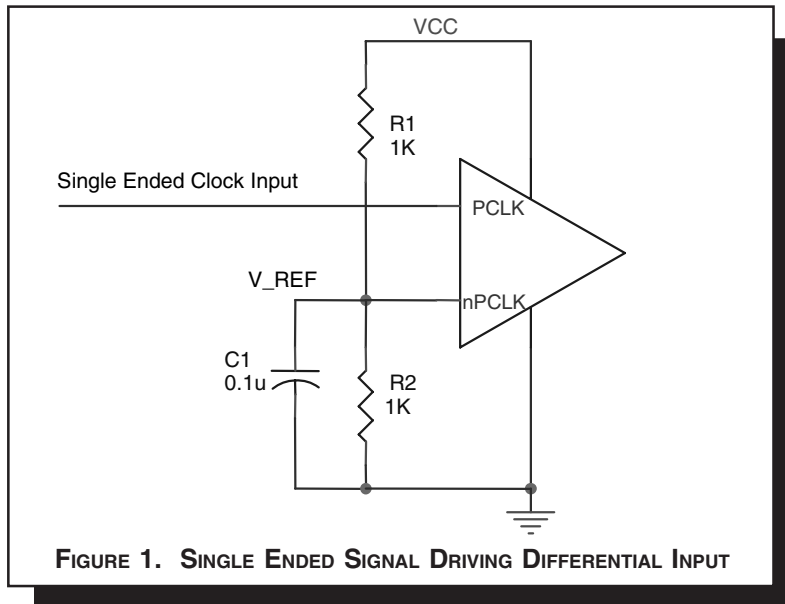


## APPLICATION INFORMATION

### WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{CC}/2$  is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin.

The ratio of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and  $V_{CC} = 3.3V$ ,  $V_{REF}$  should be 1.25V and  $R2/R1 = 0.609$ .



### RECOMMENDATIONS FOR UNUSED OUTPUT PINS

#### OUTPUTS:

##### LVPECL OUTPUT

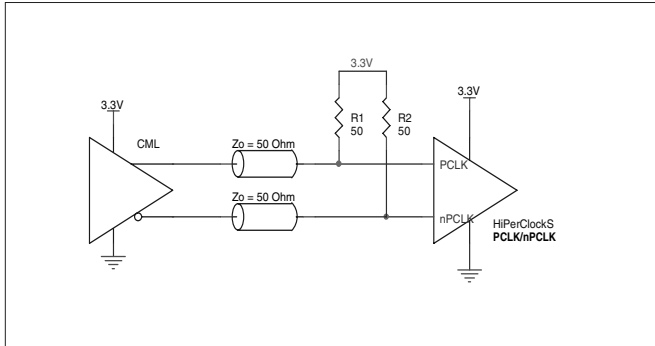
All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.



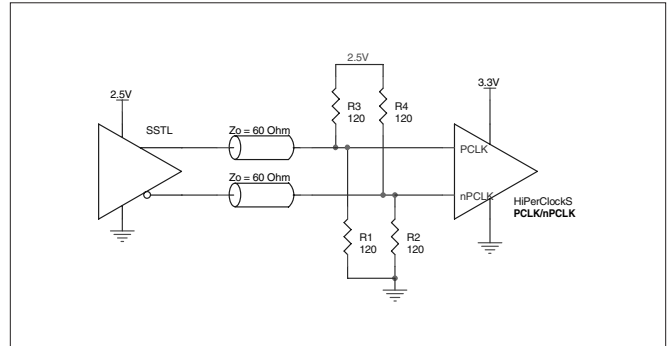
**LVPECL CLOCK INPUT INTERFACE**

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both  $V_{SWING}$  and  $V_{OH}$  must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figures 2A to 2E show interface examples for the HiPerClockS PCLK/nPCLK input driven by the most common driver types. The input interfaces sug-

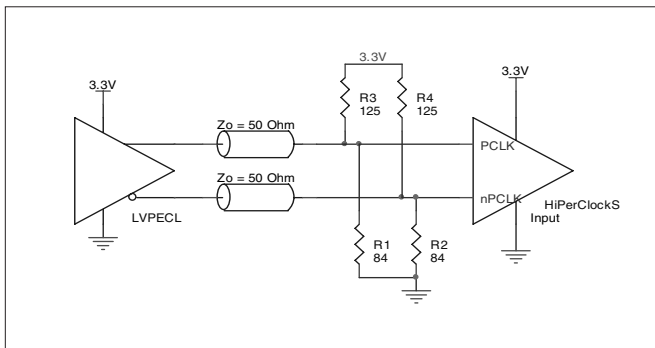
gested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.



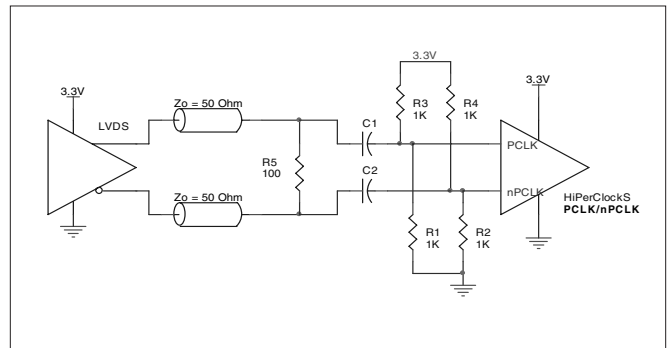
**FIGURE 2A. HiPerClockS PCLK/nPCLK INPUT DRIVEN BY A CML DRIVER**



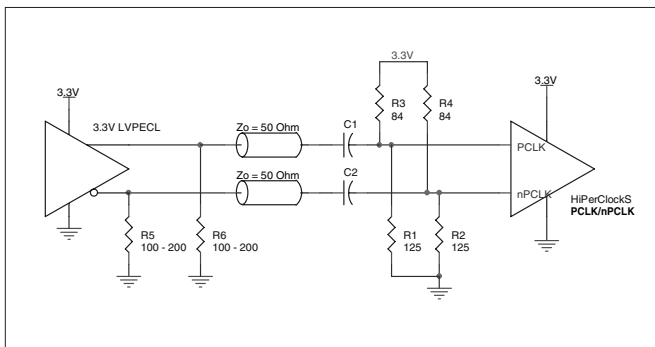
**FIGURE 2B. HiPerClockS PCLK/nPCLK INPUT DRIVEN BY AN SSTL DRIVER**



**FIGURE 2C. HiPerClockS PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER**



**FIGURE 2D. HiPerClockS PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVDS DRIVER**



**FIGURE 2E. HiPerClockS PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER WITH AC COUPLE**





### TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are

designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

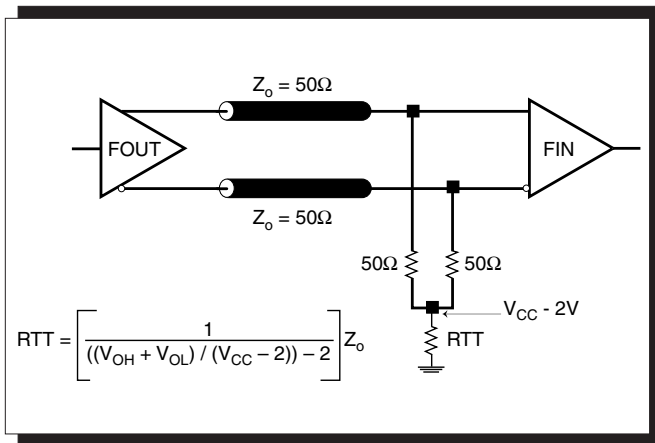


FIGURE 3A. LVPECL OUTPUT TERMINATION

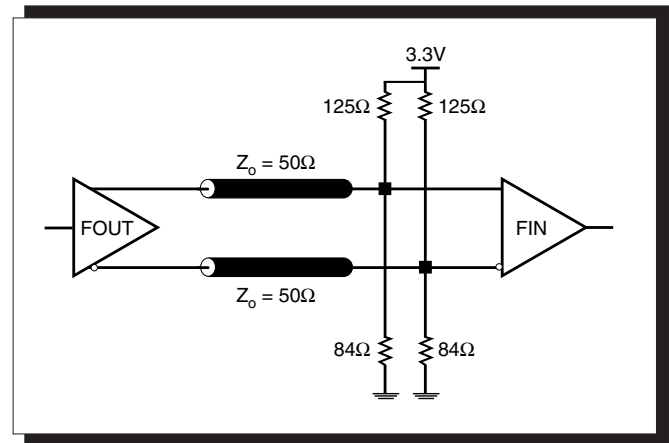


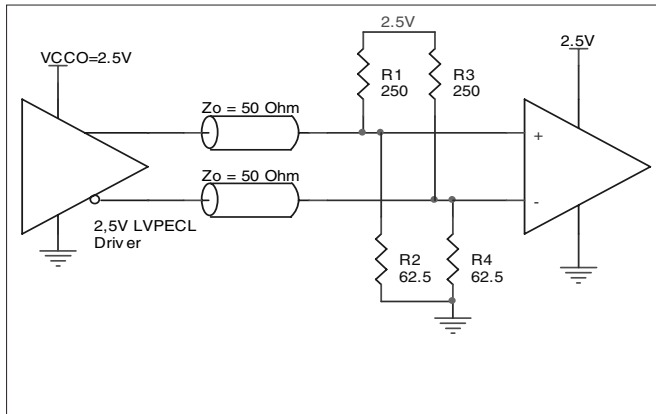
FIGURE 3B. LVPECL OUTPUT TERMINATION



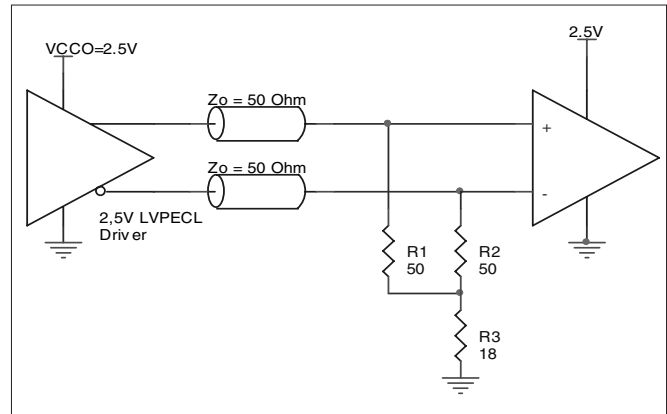
**TERMINATION FOR 2.5V LVPECL OUTPUT**

Figure 4A and Figure 4B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to  $V_{CC} - 2V$ . For  $V_{CC} = 2.5V$ , the  $V_{CC} - 2V$  is very

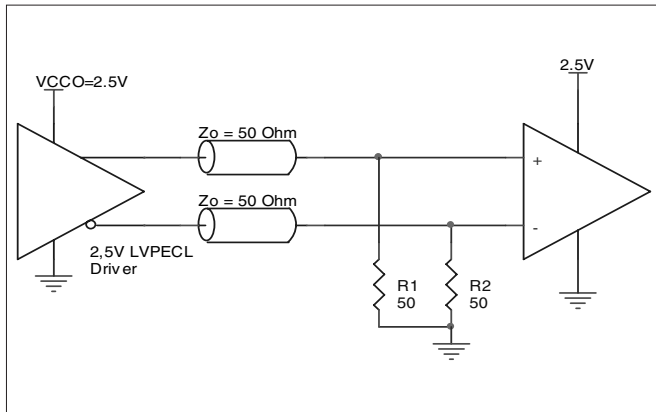
close to ground level. The R3 in Figure 4B can be eliminated and the termination is shown in Figure 4C.



**FIGURE 4A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE**



**FIGURE 4B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE**



**FIGURE 4C. 2.5V LVPECL TERMINATION EXAMPLE**



## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS853011. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS853011 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 3.8V$ , which gives worst case results.

**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{EE\_MAX} = 3.8V * 25mA = 95mW$
- Power (outputs)<sub>MAX</sub> = **30.94mW/Loaded Output pair**  
If all outputs are loaded, the total power is  $2 * 30.94mW = 61.88mW$

**Total Power<sub>MAX</sub>** (3.8V, with all outputs switching) =  $95mW + 61.88mW = 156.88mW$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 103.3°C/W per Table 5A below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ C + 0.157W * 103.3^\circ C/W = 101.2^\circ C. \text{ This is well below the limit of } 125^\circ C.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

**TABLE 5A. THERMAL RESISTANCE  $\theta_{JA}$  FOR 8-PIN SOIC, FORCED CONVECTION**

<b><math>\theta_{JA}</math> by Velocity (Linear Feet per Minute)</b>			
	<b>0</b>	<b>200</b>	<b>500</b>
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

**TABLE 5B. THERMAL RESISTANCE  $\theta_{JA}$  FOR 8-PIN TSSOP, FORCED CONVECTION**

<b><math>\theta_{JA}</math> by Velocity (Meters per Second)</b>			
	<b>0</b>	<b>1</b>	<b>2</b>
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W



3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in Figure 5.

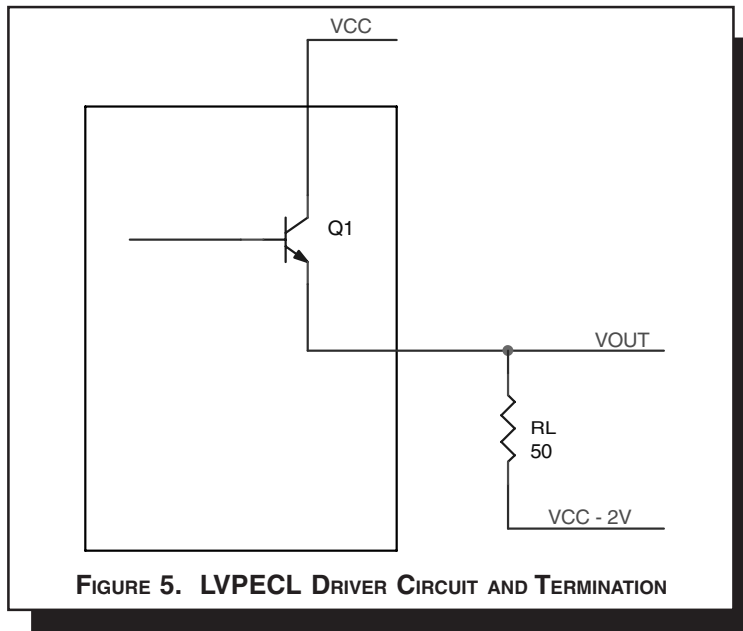


FIGURE 5. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of  $V_{CC} - 2V$ .

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{CC\_MAX} - 0.935V$

$$(V_{CC\_MAX} - V_{OH\_MAX}) = 0.935V$$

- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{CC\_MAX} - 1.67V$

$$(V_{CC\_MAX} - V_{OL\_MAX}) = 1.67V$$

$Pd\_H$  is power dissipation when the output drives high.  
 $Pd\_L$  is the power dissipation when the output drives low.

$$Pd\_H = [(V_{OH\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - 0.935V)/50\Omega] * 0.935V = 19.92mW$$

$$Pd\_L = [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - 1.67V)/50\Omega] * 1.67V = 11.02mW$$

$$\text{Total Power Dissipation per output pair} = Pd\_H + Pd\_L = 30.94mW$$



## RELIABILITY INFORMATION

**TABLE 6A.  $\theta_{JA}$  VS. AIR FLOW TABLE FOR 8 LEAD SOIC**

<b><math>\theta_{JA}</math> by Velocity (Linear Feet per Minute)</b>			
	<b>0</b>	<b>200</b>	<b>500</b>
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

**TABLE 6B.  $\theta_{JA}$  VS. AIR FLOW TABLE FOR 8 LEAD TSSOP**

<b><math>\theta_{JA}</math> by Velocity (Meters per Second)</b>			
	<b>0</b>	<b>1</b>	<b>2</b>
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W

### TRANSISTOR COUNT

The transistor count for ICS853011 is: 96

Pin compatible with MC100LVEP11 and SY100EP11U



PACKAGE OUTLINE - M SUFFIX FOR 8 LEAD SOIC

PACKAGE OUTLINE - G SUFFIX FOR 8 LEAD TSSOP

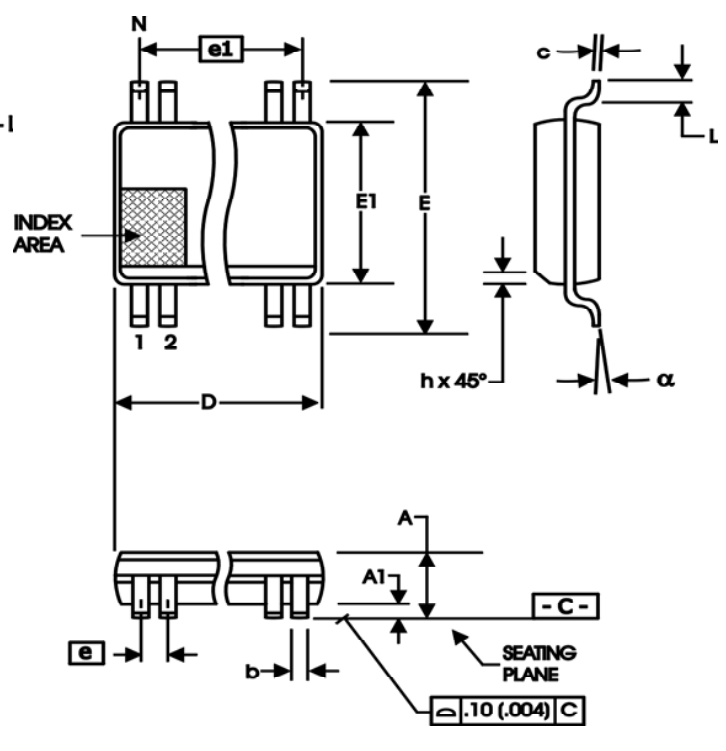
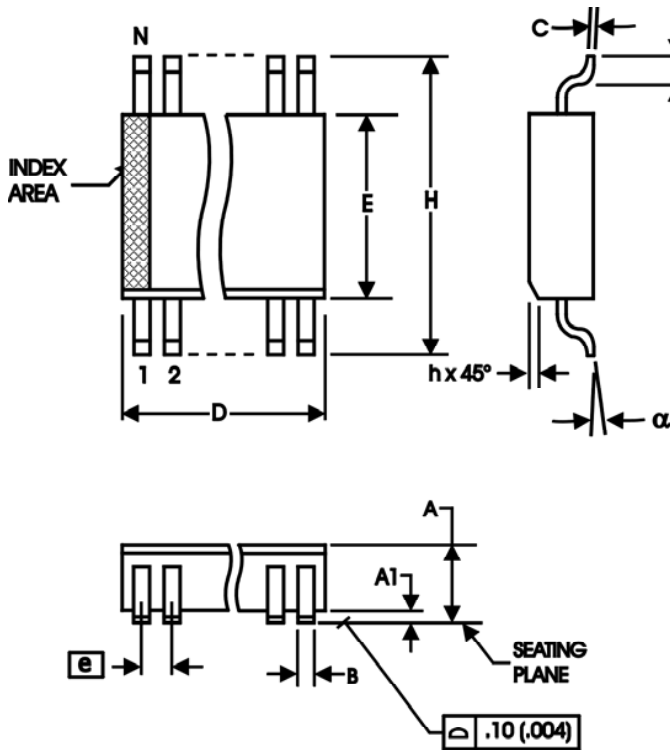


TABLE 7A. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	MINIMUM	MAXIMUM
N	8	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BASIC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
$\alpha$	0°	8°

Reference Document: JEDEC Publication 95, MS-012

TABLE 7B. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	8	
A	--	1.10
A1	0	0.15
A2	0.79	0.97
b	0.22	0.38
c	0.08	0.23
D	3.00 BASIC	
E	4.90 BASIC	
E1	3.00 BASIC	
e	0.65 BASIC	
e1	1.95 BASIC	
L	0.40	0.80
$\alpha$	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-187



**TABLE 8. ORDERING INFORMATION**

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS853011BM	853011BM	8 lead SOIC	tube	-40°C to 85°C
ICS853011BMT	853011BM	8 lead SOIC	2500	-40°C to 85°C
ICS853011BMLF	853011BL	8 lead "Lead Free" SOIC	tube	-40°C to 85°C
ICS853011BMLFT	853011BL	8 lead "Lead Free" SOIC	2500	-40°C to 85°C
ICS853011BG	011B	8 lead TSSOP	tube	-40°C to 85°C
ICS853011BGT	011B	8 lead TSSOP	2500	-40°C to 85°C
ICS853011BGLF	11BL	8 lead "Lead Free" TSSOP	tube	-40°C to 85°C
ICS853011BGLFT	11BL	8 lead "Lead Free" TSSOP	2500	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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REVISION HISTORY SHEET				
Rev	Table	Page	Description of Change	Date
B	T3B	3	3.3V LVPECL Table - changed $V_{OH}$ @ 85°, from 2.295V min. to 2.22V min. and 2.33V typical to 2.295V typical.	9/2/03
	T3C	4	2.5V LVPECL Table - changed $V_{OH}$ @ 85°, from 1.495V min. to 1.42V min. and 1.53V typical to 1.495V typical.	
	T3D	4	ECL Table - changed $V_{OH}$ @ 85°, from -1.005V min. to -1.08V min. and -- 0.97V typical to -1.005V typical.	
		6	Updated LVPECL Output Termination Diagrams.	
		8	Updated LVPECL Clock Input Interface Figure 4D.	
B		8	Corrected Figure 4C.	11/12/03
		13	Added "Lead Free" Part/Order Number rows.	
C	T4	4	AC Characteristics Table - added Additive Phase Jitter.	9/7/04
		5	Added Additive Phase Jitter Section.	
C	T8	1	Features Section - added Lead-Free bullet.	7/13/05
		10	Added "Recommendations for Unused Input and Output Pins".	
		15	Ordering Information Table - corrected Lead-Free marking and added Lead-Free note.	
C	T5B T6B	1	Pin Assignment - added 8 Lead TSSOP package.	11/2/05
		3	Absolute Maximum Ratings - added TSSOP to Package Thermal Impedance.	
		11	Power Considerations - added 8 Lead TSSOP Thermal Resistance.	
		13	Added 8 Lead TSSOP Reliability Information.	
		14	Added TSSOP Package Outline and Dimensions.	
T8	15	Ordering Information - Added 8 Lead TSSOP part number and marking.		